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LISTING OF CLAIMS:

1. (currently amended) A method for fabricating a nanoscopic transistor, comprising the steps of:

a) providing a semiconductor substrate;

b) forming a thin oxide layer on the semiconductor substrate;

c) applying a first layer of resist;

d) patterning the first layer of resist using imprint lithography to form a first pattern aligned along a first direction;

e) applying a first ion-masking material over the first pattern, and selectively lifting off the first ion-masking material to leave a first ion mask defined by the first pattern, the first ion mask ~~optionally~~ being suitable to form a gate;

f) forming first doped regions in the semiconductor substrate by implanting a suitable first dopant selectively in accordance with the first ion mask;

g) applying a second layer of resist and patterning the second layer of resist using imprint lithography to form a second pattern aligned along a second direction;

h) applying a second ion-masking material over the second pattern, and selectively lifting off the second ion-masking material to leave a second ion mask defined by the second pattern; and

i) forming second doped regions in the semiconductor substrate by implanting a suitable second dopant selectively in accordance with the second ion mask.

2. (original) The method of claim 1, wherein the second direction is substantially orthogonal to the first direction.

3. (currently amended) The method of claim 1, wherein the first ion mask is left in place after the step f) of forming ~~source and drain regions~~ first doped regions, whereby the first ion mask is suitably disposed to serve as a gate electrode.

4. (original) The method of claim 1, further comprising the step of:

j) depositing a conductive material before the step e) of applying a first ion-masking material, whereby the conductive material is patterned to serve as a gate electrode.

5. (previously amended) The method of claim 4, further comprising the step of:

k) removing the first ion mask after the step f) of forming first doped regions.

6. (previously amended) The method of claim 1, further comprising the step of:

j) removing the first ion mask after the step f) of forming first doped regions.

7. (original) The method of claim 1, wherein the semiconductor substrate is P- and the first doped regions form P++ regions suitable for isolation regions.

8. (currently amended) The method of claim 1, wherein the semiconductor substrate is P- and the second doped regions form N+ regions suitable for ~~second source and drain regions~~ second doped regions.

9. (original) The method of claim 1, wherein the smallest dimension of the first pattern is less than about one micrometer.

10. (original) The method of claim 1, wherein the smallest dimension of the second pattern is less than about one micrometer.

11. (original) The method of claim 1, wherein the smallest dimension of the first pattern and the smallest dimension of the second pattern are both less than about one micrometer.

12. (original) The method of claim 1, wherein the smallest dimension of the first doped regions is less than about one micrometer.

13. (original) The method of claim 1, wherein the smallest dimension of the second doped regions is less than about one micrometer.

14. (original) The method of claim 1, wherein the smallest dimension of the first pattern, the smallest dimension of the second pattern, the smallest dimension of the first doped regions, and the smallest dimension of the second doped regions are all less than about one micrometer.

15. (original) The method of claim 1, further comprising the step of:

forming a second gate insulated from the gate electrode and from the semiconductor substrate, the second gate being disposed between the gate electrode and the semiconductor substrate.

16. (original) The method of claim 1, wherein the steps are performed in the order recited.

17. (original) A method for fabricating an array of nanoscopic transistors, comprising the steps of claim 1, wherein the first and second patterns define a multiplicity of transistors disposed in an array.

18. (original) An integrated circuit fabricated by the method of claim 17.

19. (original) An electronic device fabricated by the method of claim 17.

20. (original) The method of claim 17, wherein the first and second patterns further define a plurality of conductive interconnections, the method further comprising the step of:

selectively severing the conductive interconnections to selectively subdivide the array of nanoscopic transistors into cells.

21 – 24. (cancelled)

25. (previously added) A method for fabricating a nanoscopic transistor, comprising the steps of:

forming an oxide layer on a semiconductor substrate;
forming a first layer of resist over the oxide layer;
imprinting a first pattern on the first layer of resist to expose first areas of the first oxide layer aligned along a first direction;
covering the patterned first layer of resist and exposed first areas of the first oxide layer with a first ion-masking material;
selectively removing first ion-masking material to leave a first ion mask defined by the first pattern on the first oxide layer;
doping regions in the semiconductor substrate not covered by the first ion mask;
forming a second layer of resist over the structure previously formed;

imprinting a second pattern on the second layer of resist to expose second areas of the first oxide layer aligned along a second direction different from the first direction;

covering the patterned second layer of resist and the exposed second areas of the first oxide layer with a gate electrode material; and

selectively removing gate electrode material to leave a gate electrode defined by the second pattern on the first oxide layer.

26. (previously added) The method of claim 25, wherein the semiconductor substrate is

doped to a first conductivity type and the step of doping regions in the semiconductor substrate comprises doping regions in the semiconductor substrate to a second conductivity type opposite the first conductivity type.

27. (previously added) The method of claim 25, wherein the semiconductor substrate is

doped to a first conductivity type and the step of doping regions in the semiconductor substrate comprises implanting a first dopant having the first conductivity type into first regions in the semiconductor substrate.

28. (previously added) The method of claim 26, further comprising, after selectively removing gate electrode material to leave a gate electrode defined by the second pattern on the first oxide layer, implanting a second dopant having a second conductivity type opposite the first conductivity type into second regions of the semiconductor substrate adjacent to the gate electrode and overlapping the first regions of the semiconductor substrate.